WHAT IS CLAIMED IS:

1. A method of forming a fin-shaped channel region, the method comprising:

providing a compound semiconductor layer above an insulating layer;

providing a trench in the compound semiconductor layer;

providing a strained semiconductor layer above the compound semiconductor layer and within the trench, the trench being associated with the fin-shaped channel region;

removing the strained semiconductor layer from above the compound semiconductor layer, thereby leaving the strained semiconductor layer within the trench; and

removing the compound semiconductor layer to leave the strained semiconductor layer and form the fin-shaped channel region.

2. The method of claim 1, further comprising providing an oxide material adjacent lateral sidewalls of the fin shaped channel region.

3. The method of claim 2, further comprising:

providing a gate conductor over the oxide material.

4. The method of claim 1, wherein the fin-shaped channel region includes silicon (Si).

5. The method of claim 4, wherein compound semiconductor layer is a silicon germanium layer.

6. The method of claim 4, wherein the first removing step is a polishing step.

7. The method of claim 6, wherein the second removing step is an etching step selective to silicon germanium.

8. The method of claim 1, wherein the second removing step utilizes a mask, the mask protecting portions of the compound semiconductor layer for a source region and a drain region.

9. The method of claim 1, wherein the fin-shaped channel region has an aspect ratio of between approximately 4 and 6.

10. A method of FinFET channel structure formation, the method comprising:

providing a first layer above an insulating layer above a substrate, the first layer including silicon and germanium;

providing an aperture in the first layer, the aperture extending to the insulating layer;

providing a strained material within the aperture; and

removing the first layer to leave the strained material.

11. The method of claim 10, wherein the removing step is an etching step selective to silicon germanium.

12. The method of claim 10, wherein the strained material is provided by selective silicon epitaxy.

13. The method of claim 10, further comprising forming a gate dielectric structure along sidewalls and a top of the strained material.

14. The method of claim 13, wherein the strained material is provided above the first layer.

15. The method of claim 14, wherein strained material is removed from above the first layer by a chemical mechanical polish step.

16. The method of claim 15, wherein the first layer is protected by a mask during the removing step at a source location and a drain location.

17. A method of fabricating an integrated circuit including a fin-based transistor, the method comprising steps of:

providing an insulative material;

providing a strain inducing layer above the insulative material;

providing an aperture in the strain inducing layer;

forming a strained material in the aperture by selective epitaxial growth;

removing at least a portion of the strain inducing layer to thereby leave the strained material as a fin structure; and

providing a gate structure for the fin structure.

18. The method of claim 17, wherein the aperture is between approximately 20 and 120nm wide.

19. The method of claim 17, wherein the removing step is a dry etching step selective to silicon germanium with respect to silicon.

20. The method of claim 17, wherein the gate structure includes polysilicon.